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Title of the Invention	Liquid Crystal Display Device
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Inventor(s):	Masuyuki Ota, Kazuhiko Yanagawa, Keiichiro Ashizawa, Yasuyuki Mishima, Kazuhiro Ogawa, Masato Oe, Katsumi Kondo and Masahiro Yanai
Applicant(s):	HITACHI LTD.

(transliterated, therefore the spelling might be incorrect)

(Partial translation)
(1)
[0023] <<Configuration of Cross-section of Matrix Portion (Pixel Part)>> Fig. 2 is a view showing a cross-section

along cutting plane line 3-3 of Fig. 1, Fig. 3 is a cross-sectional view showing a thin film transistor TFT alone cutting plane line 4-4 of Fig. 1 and Fig. 4 is a view showing a cross-section of a storage capacitor Cstg along cutting plane 5-5 of Fig. 1. As shown in Figs. 2 to 4, thin film transistor TFT, storage capacitor Cstg and a group of electrodes are formed on the lower transparent glass substrate SUB1 side of a liquid crystal layer LC and a color filter FIL and a black matrix pattern BM for blocking light are formed on the upper transparent glass substrate SUB2 side.

[0024] In addition, orientation films ORI1 and ORI2 for controlling the initial orientation of the liquid crystal are provided on the inner surfaces (liquid crystal LC side) of transparent glass substrates SUB1 and SUB2 respectively, and polarizing plates of which the polarization axes are arranged so as to be perpendicular to each other (cross nicol arrangement) are provided on the external surfaces of transparent glass substrates SUB1 and SUB2.

[0025] <<TFT Substrate>> First, a configuration of the lower transparent glass substrate SUB1 side (TFT substrate) is described in detail.

[0026] <<Thin Film Transistor TFT>> A thin film transistor TFT operates in a manner where the channel resistance between the source and the drain becomes small when a positive bias is applied to gate electrode GT and the channel resistance becomes great when the bias becomes zero.

[0027] Thin film transistor TFT, as shown in Fig. 3, has gate electrode GT, a gate insulating film GI, an i type semiconductor layer AS made of an i type (intrinsic type: no impurities for determining the conductivity type are

not doped) amorphous silicon (Si), a pair of source electrode SD1 and drain electrode SD2. Here, the source and the drain are essentially determined depending on the bias polarity between them and it should be understood that in the circuit of this liquid crystal display, the polarity between the source and the drain is inverted during the operation and, therefore, the source and the drain are switched during the operation. However, in the following description, for the purpose of convenience, one is fixed as the source and the other is fixed as the drain.

[0028] <<Gate Electrode GT>> Gate electrode GT is formed so as to be connected to a scanning signal line GL and a part of scanning signal line GL becomes gate electrode GT in the configuration. Gate electrode GT is a portion of thin film transistor TFT that is located above the active region of the transistor and is formed to be larger than i type semiconductor layer AS in order to completely cover the layer (as viewed from below). As a result of this, gate electrode GT is arranged so as to prevent i type semiconductor layer AS from being irradiated with external light or back light in addition to its original function as the gate electrode. In the present example, gate electrode GT is formed of a conductive film g1 which is a single layer. An aluminum (Al) film formed by means of sputtering, for example, is used as conductive film g1 and an anodized film AOF of Al is provided on top of conductive film g1.

[0029] <<Scanning Signal Line GL>> Scanning signal line GL is formed of conductive film g1. This conductive film g1 of scanning signal line GL is formed in the same manufacturing process as that for conductive film g1 of gate electrode GT and is formed to be integrated with conductive film g1 of gate electrode GT. A gate voltage Vg

is supplied to gate electrode GT from an external circuit by means of this scanning signal line GL. In addition, an anodized film AOF of Al is provided on top of scanning signal line GL. Here, the portion that crosses an image signal line DL is narrowed in order to reduce the probability of short circuiting with image signal line DL and is forked so that, even if it is short circuited, the short circuited portion can be separated by means of laser trimming.

[0030] <<Opposite Electrode CT>> An opposite electrode CT is formed of conductive film g1 which is the same layer as gate electrode GT and scanning signal line GL. In addition, an anodized film AOF of Al is provided on opposite electrode CT. Opposite electrode CT is completely covered with anodized film AOF and, therefore, even in the case where opposite electrode CT comes very close to an image signal line, no short circuiting occurs. In addition, opposite electrode CT and an image signal line may cross each other in the configuration. Opposite electrode CT is formed so that an opposite voltage Vcom can be applied to opposite electrode CT. In the present embodiment, opposite voltage Vcom is set at a potential that is lower than the intermediate direct current potential between the driving voltage Vdmin at the minimum level that is applied to image signal line DL and the driving voltage Vdmax at the maximum level by the field through voltage ΔVs that occurs when thin film transistor element TFT is turned to the OFF condition, and in the case where the power supply voltage to the integrated circuit that is utilized in the image signal driving circuit is desired to be reduced to approximately half, an alternating current voltage may be applied.

[0031] <<Opposite Voltage Signal Line CL>> An opposite

voltage signal line CL is formed of conductive film g1. Conductive film g1 of this opposite voltage signal line CL is formed in the same manufacturing process as that for conductive film g1 of gate electrode GT, scanning signal line GL and opposite electrode CT and is formed so as to be integrated with opposite electrode CT. Opposite voltage Vcom is supplied to opposite electrode CT from an external circuit by means of this opposite voltage signal line CL. In addition, an anodized film AOF of Al is provided on opposite voltage signal line CL. Here, the portion that crosses an image signal line DL is narrowed in the same manner as scanning signal line GL in order to reduce the probability of short circuiting with image signal line DL and is forked so that, even if it is short circuited, the short circuited portion can be separated by means of laser trimming.

[0032] <<Insulating Film GI>> Insulating film GI is utilized in thin film transistor TFT as a gate insulating film for providing an electrical field to semiconductor layer AS together with gate electrode GT. Insulating film GI is formed as a layer above gate electrode GT and scanning signal line GL. A silicon nitride film that is formed according to a plasma CVD, for example, is selected as insulating film GI, which is formed so as to have a thickness from 1200Å to 2700Å (in the present embodiment, approximately 2400Å). Gate insulating film GI is formed so as to surround the entirety of matrix portion AR and the peripheral portion is removed so as to expose external connection terminals DTM and GTM. Insulating film GI contributes to an electrical insulation of image signal line DL from scanning signal line GL and opposite voltage signal line CL.

[0033] <<I Type Semiconductor Layer AS>> I type

semiconductor layer AS is formed of amorphous silicon so as to have a thickness of 200Å to 2200Å (in the present embodiment, a film thickness of approximately 2000Å). Layer d0 is an N(+) type amorphous silicon semiconductor layer into which phosphorous (P) is doped for an ohmic contact and remains only in portions below which i type semiconductor layer AS is located and above which conductive layer d1 (d2) is located.

[0034] I type semiconductor layer AS is also provided between scanning signal line GL and image signal line DL as well as between opposite voltage signal line CL and image signal line DL at respective intersections (crossover portions). I type semiconductor layer AS at these intersections reduces short circuiting between scanning signal line GL and image signal line DL as well as between opposite voltage signal line CL and image signal line DL at the intersections.

[0035] <<Source Electrode SD1 and Drain Electrode SD2>> Source electrode SD1 and drain electrode SD2 are both formed of conductive film d1 that makes contact with N(+) type semiconductor layer d0 and of conductive film d2 formed on conductive film d1.

[0036] A chromium (Cr) film that is formed by means of sputtering is used as conductive film d1 which is formed so as to have a thickness of 500Å to 1000Å (in the present embodiment, approximately 600Å). In the case where the Cr film is formed so as to have a great thickness, the stress becomes great and, therefore, the Cr film is formed so as to have a film thickness in a range that does not exceed approximately 2000Å. The Cr film is utilized for the purpose of enhancing adhesion to N(+) type semiconductor layer d0 and of preventing Al in conductive film d2 from diffusing into N(+) type semiconductor layer d0 (as a so

called barrier layer). A film of a metal (Mo, Ti, Ta or W) having a high melting point or a silicide film ($MoSi_2$, $TiSi_2$, $TaSi_2$ or WSi_2) of a metal having a high melting point in addition to the Cr film may be used as conductive film d1.

[0037] Conductive film d2 is formed by means of sputtering of Al so as to have a thickness of 3000Å to 5000Å (in the case of the present embodiment, approximately 4000Å). An Al film has a low stress in comparison with a Cr film and, therefore, it is possible to form a thick Al film so that the resistance values of source electrode SD1, drain electrode SD2 and image signal line DL can be reduced, and such an Al film allows for the connection without fail along the steps due to gate electrode GT and i type semiconductor layer AS (improving step coverage).

[0038] Conductive film d1 and conductive film d2 are patterned using the same mask pattern, and after that, N(+) type semiconductor layer d0 is removed using the same mask or using conductive film d1 and conductive film d2 as a mask. That is to say, the portion of N(+) type semiconductor layer d0 that has remained on i type semiconductor layer AS, other than the portion beneath conductive film d1 and conductive film d2 is removed in a self-aligned manner. At this time, N(+) type semiconductor layer d0 is etched so that the entire thickness thereof is removed, and therefore, the surface portion of i type semiconductor layer AS is slightly etched, and the degree of the etching can be controlled through the etching time.

[0039] <<Image Signal Line DL>> Image signal line DL is formed of second conductive film d2 and third conductive film d3, which are the same layers as source electrode SD1 and drain electrode SD2. In addition, image signal line DL is formed so as to be integrated with drain electrode SD2.

[0040] <<Pixel Electrode PX>> Pixel electrode PX is formed of second conductive film d2 and third conductive film d3, which are the same layers as source electrode SD1 and drain electrode SD2. In addition, pixel electrode PX is formed so as to be integrated with source electrode SD1.

[0041] <<Storage Capacitor Cstg>> Pixel electrode PX is formed so that the end of pixel electrode PX on the side opposite to the end that is connected to thin film transistor TFT overlaps opposite voltage signal line CL. This overlapping forms storage capacitor (electrostatic capacitative element) Cstg having pixel electrode PX as one electrode PL2 and opposite voltage signal CL as the other electrode PL1. The dielectric film of this storage capacitor Cstg is formed of insulating film GI, which is utilized as the gate insulating film of thin film transistor TFT, and of anodized film AOF.

[0042] As shown in Fig. 1, storage capacitor Cstg is formed in a portion where the width of conductive film g1 of opposite voltage signal line CL becomes greater in the plan view.

[0043] In this case, the electrode which is positioned beneath insulating film GI in this storage capacitor Cstg is formed of Al material, and the surface of this material is anodized, and therefore, a storage capacitor can be gained where harmful effects due to dot defects (short circuiting with the electrode positioned above) caused by so-called whiskers or the like of Al barely occur.

[0044] <<Protective Film PSV1>> Protective film PSV1 is provided on thin film transistor TFT. Protective film PSV1 is formed primarily in order to protect thin film transistor TFT from moisture or the like, and material having a high transparency and high resistance to moisture is utilized for the protective film. Protective film PSV1

is formed of a silicon oxide film or a silicon nitride film in, for example, a plasma CVD unit, so as to have a film thickness of approximately 1 μm.

[0045] Protective film PSV1 is formed so as to surround the entirety of matrix portion AR, and is removed in the peripheral portion so as to expose external connection terminals DTM and GTM. As for the thicknesses of protective film PSV1 and gate insulating film GI, the former is made thick, in consideration of protective effects, while the latter is made thin, in consideration of mutual conductance gm of the transistor. Accordingly, protective film PSV1 having high protective effects is formed so as to be greater than gate insulating film GI, in order to protect as wide range as possible, including the peripheral portion.

[0046] <<Color Filter Substrate>> Next, returning to Figs. 1 and 2, the configuration on the upper transparent glass substrate SUB2 side (color filter substrate) is described in detail.

[0047] <<Light Blocking Film BM>> Light blocking film BM (so-called black matrix) is formed on the upper transparent glass substrate SUB2 side, in order to prevent light that has transmitted through unnecessary gaps (gaps other than those between pixel electrode PX and opposite electrode CT) from emitting from the display side and decreasing the contrast ratio or the like. Light blocking film BM serves as a film that prevents external light or backlight from entering into i type semiconductor layer AS. That is to say, i type semiconductor layer AS of thin film transistor TFT is sandwiched between light blocking film BM and large gate electrode GT, which are respectively located above and below i type semiconductor layer AS, and is not irradiated with external natural light or backlight.

[0048] The inside of each of the closed polygonal borders of light blocking film BM shown in Fig. 1 indicates an opening where light blocking film BM is not formed. This pattern of the borders is an example, and in the case where each opening is made greater, a pattern as that shown in Fig. 19 may be used. The direction of the electrical field is disturbed in the region of A in Fig. 19, and the display in this portion corresponds to image information within a pixel in a one-on-one manner, and indicates black in the case of black and white in the case of white, making it possible to be utilized as a display portion. In addition, the border lines in the upward and downward direction in the figure are determined by the precision of the overlapping of upper and lower substrates, and in the case where the overlapping precision is better than the electrode width of opposite electrode CT that is adjacent to image signal line DL, the openings can be enlarged when they are set in the width of the opposite electrode.

[0049] Light blocking film BM is a shield against light and is formed of a film having high insulating properties in order to prevent the electrical field between pixel electrode PX and opposite electrode CT from being influential. By having such a configuration, the electrical field parallel to the substrate surface is effectively applied to the liquid crystal layer so that an increase in the voltage that drives the liquid crystal can be suppressed. As the material of this light blocking film BM, for example, a resist material into which a black pigment is mixed is used in a manner where the film is formed so as to have a thickness of approximately 1.2 μm. In addition, a resist material into which palladium and Ni that has been electroless plated are mixed can be utilized

in another embodiment.

[0050] Then, in such a case, the interval between pixel electrode PX and opposite electrode CT can be enlarged to a certain extent, and therefore, effects can be gained where an increase in the opening ratio is achieved.

[0051] Light blocking film BM is formed in grid form around the respective pixels, in a manner where this grid partitions the effective display region into respective pixels. Accordingly, the border of each pixel is clarified by light blocking film BM. That is to say, light blocking film BM has two functions: as a black matrix and as a light blocker for i type semiconductor layer AS.

[0052] Light blocking film BM is formed in the peripheral portion in frame form, and the pattern thereof is formed so as to continue to the pattern of the matrix portion shown in Fig. 1, where a plurality of openings in dot form is provided. Light blocking film BM in the peripheral portion extends to the outside of seal portion SL, preventing leaked light caused in the device on which the display is mounted, such as a personal computer, from entering into the matrix portion. On the other hand, this light blocking film BM is held approximately 0.3 mm to 1.0 mm inside the frame of substrate SUB2, and is formed avoiding the cutting region of substrate SUB2.

[0053] <<Color Filter FIL>> Color filter FIL is formed in stripes where red, green and blue are repeated in positions that face pixels. Color filter FIL is formed so as to overlap the edge portions of light blocking film BM.

[0054] Color Filter FIL can be formed in the following manner. First, a colored base material such as an acryl-based resin is formed on the surface of upper transparent glass substrate SUB2, and the colored base material in regions other than red filter formation regions is removed

by means of a photolithographic technology. After this, the colored base material is dyed with a red dye, on which fixing treatment is carried out, so as to form red filters R. Next, by carrying out similar processes, green filters G and blue filters B are formed in sequence.

[0055] <<Overcoat Film OC>> Overcoat film OC is provided in order to prevent the dyes of color filter FIL from leaking to liquid crystal LC, and in order to flatten the steps resulting from color filter FIL and light blocking film BM. Overcoat film OC is formed of a transparent resin material such as, for example, an acryl resin or an epoxy resin.

[0056] <<Liquid Crystal Layer and Polarizing Plate>> Next, the liquid crystal layer, the orientation film, the polarizing plate and the like are described.

[0057] <<Liquid Crystal Layer>> As liquid crystal material LC, nematic liquid crystal of which the dielectric constant anisotropy Δe is positive with a value of 13.2 and of which the refraction index anisotropy Δn is 0.081 (589 nm, 20 °C), or nematic liquid crystal of which the dielectric constant anisotropy Δe is negative with a value of -7.3 and of which the refraction index anisotropy Δn is 0.053 (589 nm, 20°C) is used. The thickness (gap) of the liquid crystal layer exceeds 2.8 μm and is less than 4.5 μm in the case where the dielectric constant anisotropy Δe is positive. This is because when retardation $\Delta n \cdot d$ exceeds 0.25 μm and is less than 0.32 μm, transmittance characteristics are gained where there is almost no wavelength dependency within the range of visible light, and the major portion of the liquid crystal of which the dielectric constant anisotropy Δe is positive has a refraction index anisotropy Δn which exceeds 0.07 and is less than 0.09. On the other hand, in the case where the

dielectric constant anisotropy Δe is negative, the thickness (gap) of the liquid crystal layer is set at a value that exceeds 4.2 μm and is less than 8.0 μm. The purpose of this is to restrict retardation Δn · d to a value that exceeds 0.25 μm and is less than 0.32 μm in the same manner as the liquid crystal of which the dielectric constant anisotropy Δe is positive, and such a restriction becomes necessary because the major portion of the liquid crystal of which the dielectric constant anisotropy Δe is negative has a refraction index anisotropy Δn which exceeds 0.04 and is less than 0.06.

[0058] In addition, the below described combination of the orientation films and the polarizing plates makes it possible to gain maximum transmittance when the liquid crystal molecules rotate 45 ° in the direction of the electrical field from the direction of rubbing.

[0059] Here, the thickness (gap) of the liquid crystal layer is controlled by the size of the polymer beads.

[0060] Here, liquid crystal material LC is not particularly limited, as long as it is nematic liquid crystal. In addition, the greater the value of the dielectric constant anisotropy Δe is, the further the driving voltage can be reduced. In addition, the smaller the refraction index anisotropy Δn is, the greater the thickness (gap) of the liquid crystal layer can be made, so that the time for sealing liquid crystal can be shortened and the dispersion of the gap can be reduced.

[0061] <<Orientation Film>> Polyimide is used for orientation films ORI. The rubbing directions RDR for upper and lower substrates are parallel to each other, and the angle formed between the rubbing directions and applied electrical field direction EDR is set at 75 °. Fig. 20 shows this relationship.

[0062] Here, the angle formed between rubbing direction RDR and applied electrical field direction EDR may be set at an angle that is not less than 45 ° and less than 90 ° in the case where the dielectric constant anisotropy Δe of the liquid crystal material is positive, and may be set at an angle that exceeds 0 ° and is not greater than 45 ° in the case where the dielectric constant anisotropy Δe of the liquid crystal material is negative.

[0063] <<Polarizing Plate>> G1220DU manufactured by Nitto Denko Corporation is used as polarizing plates POL where polarized transmission axis MAX1 of lower polarizing plate POL1 are made to agree with rubbing direction RDR, and polarized transmission axis MAX2 of upper polarizing plate POL2 is made to be perpendicular to polarized transmission axis MAX1. Fig. 20 shows this relationship. As a result of this, normally close characteristics can be gained where, as the voltage that is applied to a pixel (voltage across pixel electrode PX and opposite electrode CT) of the present invention is increased, the transmittance increases.

(2)

[0092] <<Manufacturing Method>> Next, a manufacturing method for the above described liquid crystal display on the substrate SUB1 side is described in reference to Figs. 12 to 14. Here, in the drawings, the central descriptions are abbreviations of the process names, the left side shows a cross-section of the thin film transistor TFT portion shown in Fig. 3, and the right side shows a cross-section in the vicinity of the gate terminal shown in Fig. 7, along the flow of processing. Steps A to I, excluding steps B and D, are divided corresponding to the respective

steps of photo-processing, and all of the cross-sectional diagrams of the respective steps show a stage where a photoresist is removed after the completion of the process following photo-processing. Here, "photo-processing" indicates a sequence of tasks from application of a photoresist through selective exposure utilizing a mask to development of the photoresist in the present specification, and repeated descriptions are omitted. In the following, the manufacturing method is described in accordance with the divided steps.

[0093] Step A, Fig. 12

A conductive film g1 made of Al-Pd, Al-Si, Al-Ta, Al-Ti-Ta or the like is provided on a lower transparent glass substrate SUB1 made of AN635 glass (trade name) by means of sputtering so as to have a film thickness of 3000 Å. After photo-processing, conductive film g1 is selectively etched with a mixed acid of phosphoric acid, nitric acid and glacial acetic acid. As a result of this, a gate electrode GT, a scanning signal line GL, an opposite electrode CT, an opposite voltage signal line CL, and electrode PL1, a gate terminal GTM, a first conductive layer of a common bus line CB, a first conductive layer of an opposite electrode terminal CTM, an anodized bus line SHg (not shown) for connecting gate terminal GTM, and an anodized pad (not shown) that is connected to anodized bus line SHg are formed.

[0094] Step B, Fig. 12

After the formation of an anodized mask AO by means of direct drawing, substrate SUB1 is submerged in an anodizing liquid made of a liquid that is gained by diluting a solution of 3 % of tartaric acid that has been adjusted with ammonia to have PH 6.25+/- 0.05 with an ethylene glycol solution with a ratio of 1:9, and the

formation current density is adjusted to be 0.5 mA/cm^2 (constant current formation). Next, anodizing is carried out until the formation voltage reaches the 125 V that is required in order to gain a predetermined film thickness of Al_2O_3. It is desirable to subsequently hold this condition for several tens of minutes (constant voltage formation). This is important in order to gain a uniform Al_2O_3 film. As a result of this, conductive film g1 is anodized, and anodized film AOF is formed on gate electrode GT, scanning signal line GL, opposite electrode CT, opposite voltage signal line CL and electrode PL1 so as to have a film thickness of 1800 Å.

[0095] Step C, Fig. 12

A transparent conductive film g2 made of an ITO film is provided by means of sputtering so as to have a film thickness of 1400 Å. After photo-processing, transparent conductive film g2 is selectively etched with a mixed acid liquid of hydrochloric acid and nitric acid, which is used as an etchant, and thereby, the top layer of gate terminal GTM, as well as the second conductive layers of drain terminal DTM and opposite electrode terminal CTM, is formed.

[0096] Step D, Fig. 13

An ammonium gas, a silane gas and a nitride gas are introduced into a plasma CVD unit so that an Si nitride film is provided so as to have a film thickness of 2200 Å, and a silane gas and a hydrogen gas are introduced into the plasma CVD unit so that an i type amorphous Si film is provided so as to have a film thickness of 2000 Å, and after that, a hydrogen gas and a phosphine gas are introduced into the plasma CVD unit so that an N(+) type amorphous Si film is provided so as to have a film thickness of 300 Å.

[0097] Step E, Fig. 13

After photo-processing, the N(+) type amorphous Si film and i type amorphous Si film are selectively etched by utilizing SF_5 and CCl_4 as dry etching gases, and thereby, islands of i type semiconductor layer AS are formed.

[0098] Step F, Fig. 13

After photo-processing, the Si nitride film is selectively etched by utilizing SF_5 as a dry etching gas.

[0099] Step G, Fig. 14

A conductive film d1 made of Cr is provided by means of sputtering so as to have a film thickness of 600 Å, and in addition, a conductive film d2 made of Al-Pd, Al-Si, Al-Ta, Al-Ti-Ta or the like is provided by means of sputtering so as to have a film thickness of 4000 Å. After photo-processing, conductive film d2 is etched with the same etchant as that used in step B, and conductive film d1 is etched with the same etchant as that used in step A, and thus, image signal line DL, source electrode SD1, drain electrode SD2, pixel electrode PX, electrode PL2, a second conductive layer of common bus line CB, bus line SHd for short-circuiting the third conductive layer to drain terminal DTM are formed. Next, CCl_4 and SF_5 are introduced into a dry etching unit so as to etch the N(+) type amorphous Si film, and thereby, N(+) type semiconductor layer d0 between the source and the drain is selectively removed.

[0100] Step H, Fig. 14

An ammonium gas, a silane gas and a nitrogen gas are introduced into the plasma CVD unit so that an Si nitride film is provided so as to have a film thickness of 1 μm. After photo-processing, the Si nitride film is selectively etched in accordance with a photolithographic technology where SF_5 is utilized as a dry etching gas, and thereby, a

protective film PSV1 is formed.